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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,854	07/26/2001	Christopher S. MacLellan	EMC2-086PUS	7703

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,854	MACLELLAN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-6* is/are rejected.

7)☒ Claim(s) *2 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on October 19, 2001. These drawings are acceptable.

Claim Objections

Claim 3 objected to because of the following informalities: Claim 3 line 11 "faulkt" should be "fault".

Claim 3, 4, and 6-8,are objected to because of the following informalities: The term "adapted to"(claim 3 – lines 2 and 3, claim 4 - line 4, claim 6 - lines 5 and 6, claim 7 – line 7, claim 8 – lines 13 and 23) is non functional language as described in the MPEP "The subject matter of a properly construed claim is defined by the terms that limit its scope. It is this subject matter that must be examined. As a general matter, the grammar and intended meaning of terms used in a claim will dictate whether the language limits the claim scope. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim:

(A) statements of intended use or field of use,

(B) "adapted to" or "adapted for" clauses,

(C) "wherein" clauses, or

(D) "whereby" clauses.

This list of examples is not intended to be exhaustive." MPEP 2106

Claims 7 and 8 are objected to for containing a plurality of elements or steps, which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

Claims 1, and 3-10 are objected to because of the following informalities: Antecedent basis indication by the use of the term "such". The term "such" is not a specific indication of a previously mentioned limitation and can be used as "like", "resembling", or "similar" and therefore is somewhat indefinite. The examiner suggests the use of the terms "said" or "the" which are typically used to clearly indicate antecedent basis.

Claim 1: lines 1, 2, 4, 9, and 12.

Claim 3: lines 1-4, 7, 8, and 11.

Claim 4: lines 1, 3-7, and 9.

Claim 5: lines 1, and 4-6.

Claim 6: lines 1, 5-8, 10, and 14.

Claim 7: lines 2, 4, 5, 7-9, 11, 19, and 22.

Claim 8: lines 2, 4, 6-14, 22, 27, 30, and 32.

Claim 9: line 9.

Claim 10: line 3.

Claim 8 is objected to because of the following informalities: In line 8 of claim 8 "transfer;; a memory" – duplicate semi-colons – is improper.

The examiner would like to request a thorough proofreading of all of the claims and correction of possible subject/verb agreement.

Appropriate correction is required.

Allowable Subject Matter

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7-10 would be allowable over the prior art, providing the objections to the language and format of the claims have been rectified.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 fails to define the invention in the manner required by 35 U.S.C. 112, second paragraph. The claim is indefinite as to functional or operational language. The structure, which goes to make up the device, must be clearly and positively specified. The structure must be organized and correlated in such a

manner as to present a complete operative device. The phrase "a priori unaware" used in claim 5 is not a distinct limitation. Page 11 of the present specification lines 10-25 point to two seemingly conflicting descriptions of this phrase. The common usage of "a priori" is contained in the following definition: "adj 1: involving deductive reasoning from a general principle to a necessary effect; not supported by fact; "an a priori judgment" 2: based on hypothesis or theory rather than experiment adv : derived by logic, without observed facts". The common usage of aware (unaware being the opposite) is contained in the following definition: "adj 1: (sometimes followed by `of') having or showing realization or perception; 2: bearing in mind; attentive to; 3: aware or knowing; 4: (usually followed by `of') having knowledge or understanding; 5: alert and fully informed". This usage of these words or phrase in light of the specification renders this claim indefinite and thus unsearchable. The examiner requests applicant attempt to clarify the claim and/or the specification using terminology, which is known in the art to be descriptive of the claimed invention. As presented, this claim is not searchable and will not be further treated on the merits of the claim.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The terms "anticipated" (line 7) and "unanticipated" (lines 8 and 12) are not clearly defined in the specification. Page 10 line 26 through page 11 line 23 use this terminology, however the extensive use of personification in reference to the claimed invention renders this claim

indefinite based on the claims, in light of the specification. Once the 35 U.S.C. 112, second paragraph issues of claim 5 (above) are made clear in the specification, the examiner could possibly interpret these terms as "expected" and "unexpected" and be reasonably certain of what has been claimed. However, as presented, this claim is not searchable and will not be further treated on the merits of the claim. The examiner requests applicant attempt to clarify the claim and/or the specification using terminology, which is known in the art to be descriptive of the claimed invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that

the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker U.S. Patent No. 6,539,503 in view of Williams U.S. Patent No. 6,590,929.

As per claims 1, 4 and 6, Walker substantially teaches the claimed system and methods of testing of a program or a design of an electronic device using digital logic circuitry. The method implements testing the design of software or an electronic device and injecting, after initiation of the testing step, a predetermined error pattern into a value operated upon by the design of the digital logic circuitry. The software is a simulation of the design of a processor having a cache with error detection and/or correction circuitry. A triggering condition (i.e. a cache hit) is in response to which a detectable error is injected into the cache. The simulated operations of the model are observed to determine whether the injected error is detected, as should happen if the processor's error detection circuitry has been designed properly. This device can be an apparatus, or computer software embedded on a computer readable medium, for testing a program with an error detector. The apparatus or software

contains the program, an error injector module connected to the program; and a checker module connected to the program. The checker module is capable of determining whether the program responds appropriately to an error dynamically produced by the error injector module during execution of the program. By injecting errors dynamically the system facilitates precisely focused testing at any time during simulated operation regardless of initialization conditions. (column 6 line 43 through column 7 line 50, figure 7) Not explicitly disclosed is the process of corrupting a specified bit.

However, in an analogous at, Williams teaches that in order to fully exercise the error correction path, it is not only necessary to decide "when" to inject an error along the error correction code (ECC) path, it is necessary to vary which bit has an error. In order to accomplish this, additional logic that randomly determines which bit to corrupt is joined with a controllable bit stream generator (CBSG) in order to randomly inject errors in random bits within the ECC path. *"With reference now to FIG. 5B, a circuit diagram showing data array 500 augmented with error injection logic is depicted. Combination 309 is utilized to produce controllable random bit source 304. Random bit source 304 is utilized to determine "when" an error will be injected in the ECC path. An additional LFSR 202 is utilized to generate pseudo-random numbers on signals 530. Decoder 510 takes signals 530 and produces single bit outputs 520 one and only one of which, corresponding to the random number of signals 530, is active at any given time. This logic structure serves to randomly select which data bit will be corrupted in order to test ECC logic 501. Logical AND gates 532 drive logical*

exclusive OR (XOR) gates 533 to toggle the chosen data bit at the chosen time before presentation to ECC logic 501. In this manner random bit failures at random times are effectively simulated. Structures such as shown in FIG. 5B represent a second major class of circumstances for which the present invention may be usefully employed. In such circumstances a CBSG is utilized to determine, on a controllable, randomly occurring basis, "when" a path is to be exercised. Additional logic, specific to the particular circumstance, is utilized to randomly select "how" the path is to be exercised. This structure, CBSG combined with specific logic to randomly determine how a path is exercised, provides an efficient means of exercising paths with multiple operating modes." (Column 7 line 12-46, figures 4-6) Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the bit corruption method of Williams with the error check system of Walker. This would have been obvious as suggested by William (column 7 lines 12-15) in order to fully exercise the ECC paths.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,067,647 Cummins

This patent teaches an apparatus for inserting an error signal onto a bidirectional signal line. The apparatus includes a first switch for decoupling a first terminal of the bidirectional signal line from a second terminal of the bidirectional signal line,

a second switch for coupling the error signal to the first terminal, and a third switch for coupling the error signal to the second terminal. The apparatus also includes a control unit for generating a switch enable signal. When the switch enable signal is deasserted, the first switch closes and the second and third switches open, such that the first terminal is coupled to the second terminal. When the switch enable signal is asserted, the first switch opens and the second and third switches close, such that the error signal is coupled to the first and second terminals.

U.S. Patent No. 6,604,211 Heiman et al.

This patent teaches a method and apparatus for initiating and analyzing an error recovery procedure in a data storage device. Error recovery procedures are initiated by the simulation of an injected error event onto a particular location of the storage device. The simulation is implemented by corrupting the differential read signal of the storage device prior to error detection and decoding by the storage device. The operation and control of the software error recovery analysis tool is administered through a software application offering a graphical and interactive environment for measurement and automation. The application, corruption device, and a circuit designed to operate the timing and control of the tool are linked such that communication between the components defines the invention as a whole. During the signal corruption, the application allows the monitoring of any responses to the simulated error events by the data storage device.

"Error Injection Aimed at Fault Removal in Fault Tolerance Mechanisms- Criteria for Error Selection Using Field Data on Software Faults" by Christmansson et al. Proceedings Seventh International Symposium on Software Reliability Engineering, 30 Oct.-2 Nov. 1996 pages 175 – 184 Inspec Accession Number: 5443975

This paper teaches a system in which fault injection allows a detailed study of complex interactions between faults and fault handling mechanisms. It can be a useful complement to analytical modeling and formal verification techniques in the testing of fault tolerant systems. However, work on fault injection has not matured adequately to provide industry with cost effective alternatives for the validation of fault tolerant systems. This study analyzes 408 customer discovered faults (defects) in a release of a large operating system product. We discuss methods to select the error types for an error injection experiment in the system test environment, aimed at fault removal. Using four levels of severity and a total of 24 error types as recorded in the customer defects records, we analyze the faults in terms of fault types and system test triggers as defined in ODC. Our work shows examples of criteria that can be used to select errors for injection that use the information from the field reported defects

"An Experimental Comparison of Fault and Error Injection" by Christmansson et al. Ninth International Symposium on Software Reliability Engineering, 4-7 Nov. 1998. pages 369 - 378 Inspec Accession Number: 6097082

This paper teaches that the complex interactions between faults, errors, failures and fault handling mechanisms can be studied via injection experiments. This paper presents an investigation of both fault and error injection techniques for emulating software faults. For evaluation, 1600 software faults and 5400 time-triggered errors were injected into an embedded real-time system. The cost-related results are: (i) the time required to create a fault set for fault injection was about 120 times longer than the time required to create an error set for time-triggered injection, and (ii) the execution time for the time-triggered error injection experiments was four times shorter than for the fault injection experiments. However, the error injection would be only 1.3 times faster if another strategy for fault injection had been used. Furthermore, failure symptom-related results are: (i) the test case had a greater influence than the fault type on the failure symptoms for fault injections, (ii) the error type had a greater influence on the failure symptoms for time-triggered error injections than had the test case, and (iii) the error type had a larger impact on the failure symptoms than the fault type

"*Combining Software-Implemented and Simulation-Based Fault Injection into a Single Fault Injection Method*" by Guthoff et al. Twenty-Fifth International Symposium on Fault-Tolerant Computing, 27-30 June 1995. pages 196 - 206
Inspec Accession Number: 5028555

This paper teaches thatFault/error injection has emerged as a valuable means for evaluating the dependability of a system. In particular, software-based techniques (which can be described as software-implemented and simulation-

based techniques) have become very popular because of the relative simplicity of injecting faults. After discussing the advantages and drawbacks of these techniques, two approaches are introduced which try to overcome crucial problems when using software-based fault injection techniques. The first one improves the accuracy of software-implemented fault injection experiments. The second one offers detailed insights into the system dynamics in the presence of faults. With this knowledge, the number of fault injections (a major concern in simulation-based fault injection) can be significantly reduced. These approaches can be joined together, offering accuracy of fault injection results as well as transparency of the system dynamics in the presence of faults.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CB

Cynthia Britt
Examiner
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